L Number	Hits	Search Text	DB	Time stamp
-	3	("6449741" or "6154715" or "6536006").pn.	USPAT; US-PGPUB	2004/04/19 08:08
-	1	(("6449741" or "6154715" or "6536006").pn.) and differential	USPAT; US-PGPUB	2004/04/15 14:47
-	1	(("6449741" or "6154715" or "6536006").pn.) and simultaneous	USPAT; US-PGPUB	2004/04/15 14:51
-	1	(("6449741" or "6154715" or "6536006").pn.) and concurrent	USPAT; US-PGPUB	2004/04/15 15:40
-	1	(("6449741" or "6154715" or "6536006").pn.) and evaluate	USPAT; US-PGPUB	2004/04/15 15:46
-	0	(("6449741" or "6154715" or "6536006").pn.) and evaluat	USPAT; US-PGPUB	2004/04/15 15:46
-	2	(("6449741" or "6154715" or "6536006").pn.) and evaluat$3	USPAT; US-PGPUB	2004/04/15 15:54
-	24577	test$3 and analog and digital and differential	USPAT; US-PGPUB	2004/04/15 15:55
-	410	(test$3 and analog and digital and differential) and 714/$.ccls.	USPAT; US-PGPUB	2004/04/15 15:56
-	363	((test$3 and analog and digital and differential) and 714/$.ccls.) and @ad<20010619	USPAT; US-PGPUB	2004/04/15 15:56
-	124	(((test$3 and analog and digital and differential) and 714/$.ccls.) and @ad<20010619) and (simultaneous or concurrent)	USPAT; US-PGPUB	2004/04/15 15:57
-	46	((((test$3 and analog and digital and differential) and 714/$.ccls.) and @ad<20010619) and (simultaneous or concurrent)) and evaluat$3	USPAT; US-PGPUB	2004/04/19 11:34
-	5	"differential monitoring device"	USPAT; US-PGPUB	2004/04/15 17:38
-	1	09/883,190	USPAT; US-PGPUB	2004/04/15 17:38
-	24	ltx.as.	USPAT; US-PGPUB	2004/04/19 08:09
-	16	ltx.as. and differential	USPAT; US-PGPUB	2004/04/19 08:09
-	1	6512989/.pn.	USPAT; US-PGPUB	2004/04/19 11:35

Product news
received on 1 June 2001
from **Tektronix** *(contact details)*

Digital phosphor scope improves on 2GH devices

The latest addition to the Tektronix TDS7000 Series DPO family is the 2.5GHz TDS7254.

The latest addition to the Tektronix TDS7000 Series DPO family is the 2.5GHz TDS7254, based on the sa high-performance characteristics, graphical user interface and Open Windows platform as the 4GHz TDS7404 DPO introduced last year and the world's fastest real time oscilloscope.

Using the same SiGe technology found in the TDS7404, the TDS7254 DPO is suitable for a variety of advanced test applications including signal integrity measurements and jitter and timing analysis.

"Semiconductor speeds in the newest electronics designs are driving the need for high-performance test equipment.

Our customers in the communications and computer industries are finding that the current 2GHz instruments on the market are simply not providing enough headroom to accurately measure signal integrity", said David Churchill, vice president, Instrumentation Business Unit, Tektronix.

"The TDS7254 fills that performance gap, and provides what is believed to be the most accurate representation circuit behaviour available at an excellent value for customers who don't need the premium performance of the TDS7404 DPO".

As clock frequencies in the computer and communications industries continue to climb, signal integrity and timin margin issues have become crucial.

The TDS7254 leverages the TekConnect signal interconnect system to fully address signal integrity analysis, ev when dealing with the 200ps edges typical of today's high speed components.

An option available with this system includes the 4GHz (120ps risetime) P7240 active probe and the 3GHz (130 risetime) P7330 differential probe.

The P7330 provides direct access to differential signals such as LVDS and similar technologies without requirin the user to dedicate two scope channels.

The 20Gsample/s real-time sample rate and delta-time measurement precision deliver superb jitter analysis results.

Measurements can be made on differential signals and between two separate input channels.

Comprehensive statistics and histograms of the timing parameters, and also trend plots, enhance its powerful analysis capabilities.

Pioneered by Tektronix, the first DPO was introduced in June 1998 as a new approach to signal acquisition.

The DPO architecture dedicates unique ASIC hardware to capture signal data at over 400,000 waveforms per second, giving design engineers an unmatched ability to view signals and circuit behaviour.

Based on an Open Windows platform, this innovative instrument offers unprecedented customisation and extensibility using Windows-compatible hardware and software, including third-party analysis tools.

The TDS7254 DPO provides engineers with advanced test capabilities for verification, debug and characterisati of sophisticated electronic designs.

Classic analogue-style controls, large touch-sensitive display and graphical menus provide intuitive control.

Standard interfaces allow expansion of the TDS7254 to include peripherals such as storage devices, a modem, a wireless LAN connection.

Once networked, users can share files with team members worldwide, access print resources, reference design data via the Web, and exchange e-mail.

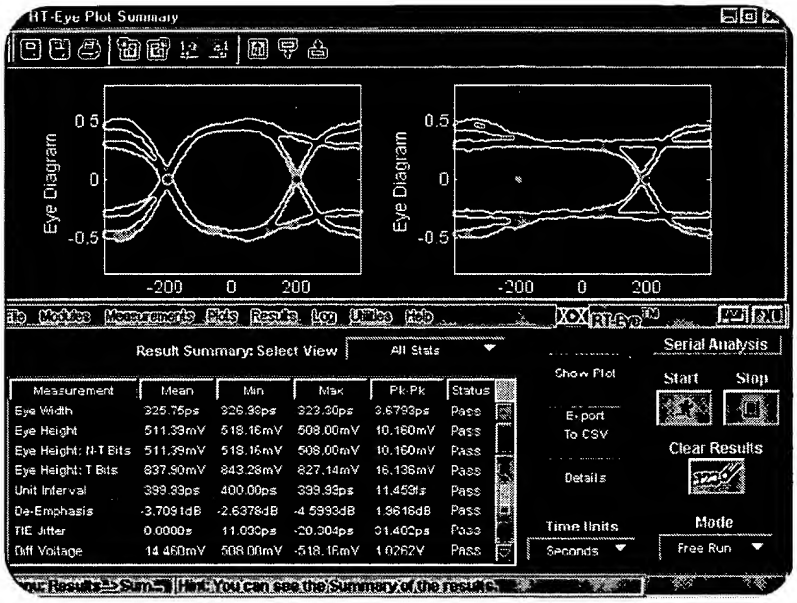
And, using the dual-monitor mode supported by Windows, designers can refer to and exchange this critical information while simultaneously making measurements on any of the TDS7000 Series.

More information:

[redacted]
- See contact details for Tektronix and other news
- Email this news to a colleague

RT-Eye™ Serial Data Compliance and Analysis Software

▶ TDSRT-Eye



Accurate, Simple and Customizable Physical Layer Testing on Emerging Serial Data Standards Up to 3.2 Gb/s

When designing to industry standards, analog validation and compliance testing is critical to ensure device interoperability. RT-Eye Serial Data Compliance and Analysis software (Opt RTE) used with the TDS/CSA7000 and TDS6000 series of high-performance oscilloscopes, and proper probing solutions, provides the complete solution for analog validation and compliance testing of serial data buses.

▶ Applications

Analog Validation and Compliance Testing of Emerging Serial Data Standards Including:

- PCI Express
- InfiniBand
- Serial ATA
- Fibre Channel
- 10 GbE XAUI
- 10 GbFC XAUI
- IEEE 1394b
- RapidIO

▶ Features & Benefits

Real Time Acquisition and Analysis on Electrical Standards Up to 3.2 Gb/s

Real Time Eye (RT-Eye) Clock Recovery and Eye Rendering Provides:
- High Precision Eye Diagrams and Accurate Jitter Measurements*1
- Standard Specific Clock Recovery
- Pattern Length Verification for Jitter Measurement
- De-emphasis Measurements

Selectable Clock Recovery Algorithms That Model Receiver Device Behavior

SmartGating Feature for Flexible Clock Recovery and Measurement Windowing

Amplitude, Timing, and Jitter Measurements (including RJ, DJ, and Total Jitter @ 10^{-12} BER)

Automated Pass/Fail Waveform Mask and Measurement Limit Testing

Flexible Plotting and Export Tools for Further Serial Data Analysis

Multiple Graticule Plotting Windows for Simultaneous Eye Diagram, Trend, Histogram, Spectrum, and Bathtub Curve Analysis

Limits Module Feature for Customized Compliance Testing

Compliance Modules (Optional) Provide "plug-fest" Level Compliance Tests
- Available: PCI Express (Opt. PCE), InfiniBand (Opt. IBA)
- Other Standards: Under Development

Custom and Standard Specific Report Generation

Programming Interface for Test Automation via OpenChoice™ Software (GPIB and LAN)

*1 Down to 700 fs RMS (TDS6000) and down to 1.5 ps RMS (TDS/CSA7000)

Tektronix
Enabling Innovation

Signal Integrity Starts at the Probe Tip

There are four fundamental probing approaches for high-speed signaling in differential serial buses. Active probing is required for probing live links on a circuit board. The use of two P7260 active probes provides a 6 GHz pseudo-differential solution that allows for the measurement of AC and DC common mode waveforms. The P7350 5 GHz active probe provides true differential measurement at the probe tip. For component and system compliance tests that require the serial link to be broken and terminated into 100 Ω differential, TCA-SMA connectors (provided standard on TDS6000 and TDS/CSA7000 series) provide a pseudo-differential solution. In order to take full advantage of the channel count and performance of your oscilloscope, the P7350SMA differential active probe is recommended. The P7350SMA probe provides single channel measurement for differential SMA connected test fixtures and devices, freeing up the other channels of the oscilloscope for additional testing. The P7350SMA also allows for simpler device test setup by allowing the use of a common mode termination voltage.

RT-Eye Clock Recovery and Eye Rendering

The first step in creating an eye diagram and performing accurate jitter measurements on data is recovering the clock from the serial bit stream. The RT-Eye eye rendering technique provides user selectable algorithms (PLL or Constant Clock) to recover the clock. This technique provides the following benefits:

High Precision Eye Diagrams – Since the waveform is captured from a single trigger event, and the clock is recovered through software, this method provides a much lower JNF than most Equivalent Time (ET) hardware-based clock recovery techniques.

Standard Specific Clock Recovery – PLL-based clock recovery is most common in many data communications standards. However, some standards such as PCI Express require supporting many receiver clock recovery topologies such as phase interpolation and oversampling. Software-based clock recovery allows you to select the clock recovery method that best suits your device. Further, use of the new SmartGating feature allows the user to define a "clock recovery window" within the acquisition as well as an additional "analysis window" that defines where in the recovery window the measurements will be made.

Pattern Length Verification – To perform real-time jitter measurements such as Random Jitter (RJ), Deterministic Jitter (DJ), and Total Jitter (TJ) at 10^{-12} BER, a jitter test pattern length must be specified. The RT-Eye software lets you enter a pattern length or select from a number of popular jitter test patterns such as TS1, CJTPAT, CSPAT, CRPAT, etc. The software then verifies your device is transmitting a valid pattern length for the measurement.

De-emphasis Measurements – The real-time capture provides the ability to differentiate between transition bits and trailing bits for mask testing and measurements useful in systems employing De-emphasis (form of active equalization also known as Pre-emphasis or Equalization). Amplitude measurements can be made separately on the emphasized bits and the non-emphasized bits, allowing a De-emphasis measurement ratio to be displayed.

Waveform Eye Diagrams and Jitter Measurements are Inseparable

In the past, waveform mask testing and jitter measurements have been performed with at least two and sometimes three pieces of instrumentation. Waveform eye diagrams were viewed with sequential Equivalent Time (ET) sampling oscilloscopes or real-time oscilloscopes operating in a random ET mode.

Until the recent advent of real time jitter (RJ, DJ, and TJ @ BER) methodology in TDS oscilloscopes, BERT and/or Time Interval Analyzers were required to make Total Jitter measurements, using methods developed by data communications industry groups. More recently, some standards in the computer industry, such as PCI Express and Serial ATA, require that jitter measurements be performed on a specified number of consecutive (contiguous) bits, a requirement only satisfied by real-time oscilloscope technology. Whichever jitter measurement method is required, TDS RT-Eye software performs eye diagrams and various industry-specified jitter measurements from a single real-time waveform acquisition. Additional confidence can be gained by accumulating statistics over multiple acquisitions. This allows you to use a single high-performance real-time oscilloscope for design, debug, validation, and compliance of your serial data components.

Simple and Parametric Limits Modules

Mask testing and jitter measurements performed with TDS RT-Eye software can be turned into a custom compliance test by defining a Limits File and a User Mask File. A Limits File allows you to select which measurements you want to perform Pass/Fail compliance testing on. Test limits on masks and measurements can be edited and saved into User Mask and Limits Files.

Standard-specific Compliance Modules

TDS RT-Eye software can also be configured with optional Compliance Modules. Compliance Modules provide specific Pass/Fail waveform mask and measurement limit testing performed at industry-hosted "plug-fests." Compliance Modules currently available include:

InfiniBand Compliance Module – The InfiniBand Compliance Module (Opt. IBA), when ordered with TDS RT-Eye software, provides the complete solution for electrical compliance tests. Module includes physical layer measurements called out in Chapter 6 of version 1.1 of the InfiniBand architecture specification.

PCI Express Compliance Module – The PCI Express compliance module (Opt. PCE), when ordered with TDS RT-Eye software, provides the complete solutions for electrical compliance tests. Module includes physical layer measurements called out in Section 4.3 of version 1.0a of the PCI Express Base Specification.

Custom and Standard Specific Report Generation

Whether you're documenting results in the validation stage of your design or archiving compliance reports for future reference, the TDS RT-Eye software provides both standard compliance report templates and a Report Generator that allows you to customize your test reports.

▷ Characteristics

Bit Rates Supported – Up to [oscilloscope bandwidth (GHz)/1.5] Gb/s on 8B/10B encoded copper standards.

Measurements

Timing – Eye Width, Rise Time, Fall Time, Unit Interval, Bit Rate, Differential Skew.

Amplitude – Eye Height, Differential Voltage, High Amplitude, Low Amplitude, Common Mode DC Voltage, Common Mode AC Voltage, De-Emphasis.

Jitter – Jitter @ BER (RJ, DJ, TJ, and Jitter Eye Opening for a specified Bit Error Ratio), Jitter TIE (Data Time Interval Error).

Mask and Measurement Compliance Testing (Pass/Fail) – User definable mask geometries (User Mask) and measurement limit definition (Limits File). Masks and Limits hardcoded in Compliance Modules.

Clock Recovery – PLL (fc/1667 or custom), Mean, Median, Gated.

SmartGating – Provides up to two gated regions for clock recovery and measurement results. Gating Options – Cursors, Unit Intervals, Edges.

Population Control – Halts measurement accumulation on a specified Measurement Population or Number of Acquisitions.

Plots – Define up to four plots on multiple graticules. Plots can be viewed on instrument display or second monitor. Supported Plot Types: Unit Interval, Trend, Histogram, Spectrum, Bathtub Curve.

Worst Case Waveform Logging – Provides capture of worst case waveform for specified test condition.

Remote Control for Automation – The software can be controlled over GPIB or 100BaseT LAN connection. Windows and Unix remote operation is supported.

Online Help – Provides easy reference to standard test definitions.

Tektronix Oscilloscopes Supported

TDS6000 and TDS/CSA7000 series oscilloscopes (1.5 GHz models and above).

Recommended System Requirements

- ▷ Windows 2K OS (order upgrade TDS7UP, CSA7UP, or TDS6UP Opt. W2K).
- ▷ SDRAM (order upgrade 040-1682-00, 256MB DIMM module).
- ▷ 850MHz Processor (order upgrade TDS7UP, CSA7UP, or TDS6UP Opt. CPU).
- ▷ Version 2.4 Firmware (www.tek.com/site/sw/search/).

RT-Eye™ Serial Data Compliance and Analysis Software

▶ TDSRT-Eye

▶ Ordering Information

TDSRTE

RT-Eye™ Serial Data Compliance and Analysis Software Option.

Includes: Software on a compact disk, online documentation, and quick reference guide. Five-time free trial available to all supported instrument models.

When Ordering a New Oscilloscope:

Order from the options listed below.

When Upgrading an Existing Oscilloscope:

Order TDS6UP, TDS7UP, or CSA7UP with the options listed below.

Options

Opt. RTE – RT-Eye Serial Data Analysis software for TDS6000 and TDS/CSA7000 series oscilloscopes (1.5 GHz instrument models and above).

Opt. IBA – Requires Opt. RTE. Adds InfiniBand Compliance Software Module (4 GHz instrument models and above).

Opt. PCE – Requires Opt. RTE. Adds PCI Express Compliance Software Module (4 GHz instrument models and above).

Recommended Accessories

P7350 – 5 GHz differential probe.

P7350SMA – 5 GHz SMA input differential probe.

P7260 – 6 GHz single-ended probe.

P7240 – 4 GHz single-ended probe.

TCA-BNC – TekConnect®-to-BNC adapter.

AWG710 – Arbitrary waveform generator.

DTG5274 – Data timing generator.

Test Fixtures – Refer to www.tektronix.com/serial_data for information on standard-specific test fixtures.

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Updated 20 September 2002

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Product(s) are manufactured in ISO registered facilities.

10/03 HB/SFI 55W-16615-3

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Differential Signals

The Differential Difference!

Douglas Brooks

Most of us intuitively understand the nature of a signal propagating down a wire or a trace, even though we might not be familiar with the name given to this type of wiring strategy --- single-ended mode. The term "single-ended" mode distinguishes this approach from at least two other types of signal propagation, differential mode and common mode. These latter two often seem much more complicated to people.

Differential mode: Differential mode signals propagate through a *pair* of traces. One trace carries the signal as we normally understand it, the other carries a signal that is (in theory, at least) exactly equal and opposite. Differential and single-ended modes are not quite as different as they may initially appear. Remember, ALL signals have a return. Single ended mode signals return, typically, through the zero-voltage, or ground, circuit. Each side of a differential signal ***would*** return through the ground circuit, except that since each signal is exactly equal and opposite, the returns simply cancel (with no part of them appearing on the zero-voltage or ground circuit).

Although I won't spend much time on it in this column, common-mode refers to signals that occur on **both** traces of a (differential) signal pair or on **both** the single-ended trace and ground. This is not intuitively easy for us to understand, because we have trouble envisioning how we can generate signals like that. It turns out that usually *we* don't generate common-mode signals. They are most often noise signals generated by spurious conditions within our circuit or coupled into our circuits from adjacent or outside sources. Common-mode signals are almost always "bad," and many of our design rules are designed to try to prevent them from occurring.

Routing Differential Traces: Although this may appear to be an awkward order, I am going to describe routing guidelines for differential signals before I describe the advantages of using them in the first place. Then, when I discuss the advantages (below), I will be able to explain how the guidelines relate to and support those advantages.

Most of the time (there are some exceptions), differential signals are also high-speed signals. Thus, high-speed design rules normally apply, especially with respect to designing our traces to look like transmission lines[1]. This means we must be careful to design and lay out our traces in such a way that the characteristic impedance of the trace is constant everywhere along the trace.

In laying out differential pairs, we want each individual trace to be identical to its pair. That means, to the maximum extent practical, each trace in a differential pair should have the identical impedance and should be of the identical length. Differential traces are normally routed as pairs, with the distance between them being a constant at every point along the way. Normally, we try to rout differential pairs as closely together as possible.

Differential Signal Advantages: Single-ended signals are normally referenced to some sort of "reference" level. This may be the positive or ground voltage, a device threshold voltage, or another signal somewhere. A differential signal, on the other hand, is referenced only to its pair. That is, if the voltage on one trace (+ signal) is higher than on the other trace (- signal), we have one logical state, if it is lower we have the other logical state (see **Figure 1**). This has several advantages:

(a) Timing is much more precisely defined, because it is easier to control the crossover point on a signal pair than it is to control an absolute voltage relative to some other reference. This is one of the reasons for exactly equal length traces. Any timing control we have at the source could be compromised if the signals arrive at different times at the other end. Furthermore, if signals at the far end of the pair are not exactly equal and opposite, common-mode noise might result which might then cause signal timing and EMI problems.

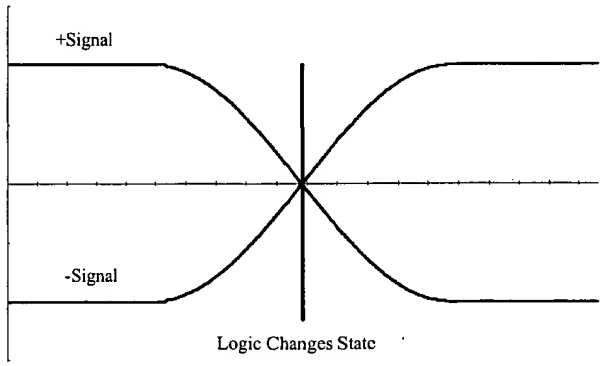

Figure 1
Logic state changes at the single point where the differential signal curves cross.

This is adapted from an article that appeared in Printed Circuit Design, a CMP publication, May, 2001

(b) Since they reference no other signals than themselves, and since the timing of signal crossover can be more tightly controlled, differential circuits can normally operate at higher speeds than comparable single-ended circuits.

(c) Since differential circuits react to the ***difference*** between the signals on two traces (whose signals are equal and opposite) the resulting net signal is twice as large, compared to ambient noise, as is either of the single-ended signals. Therefore, differential signals, all other things equal, have greater signal/noise ratios and performance.

Differential circuits are sensitive to the difference in the signal level on the paired traces. But they are (relatively) insensitive to the absolute voltage level on the traces compared to some other reference (especially ground). Therefore, differential circuits are relatively insensitive to such problems as ground bounce and other noise signals that may exist on the power and/or ground planes, and to common mode signals that may appear equally on each trace.

Differential signals are somewhat immune to EMI and crosstalk coupling. If the paired traces are routed closely together, then any externally coupled noise will be coupled into each trace of the pair equally. Thus the coupled noise becomes "common mode" noise to which the circuit is (ideally) immune. If the traces were "twisted" (as in twisted pair) the immunity to coupled noise would be even better. Since we can't conveniently twist differential traces on a PC board, placing them as close together as practical is the next best thing.

Differential pairs that are routed closely together couple closely to each other. This mutual coupling reduces EMI emissions, especially compared to single-ended traces. You can think of this as each trace radiating equal but opposite to the other, thus canceling each other out, just like signals in a twisted pair do! The more closely the differential traces are routed to each other, the greater the coupling, and the less will be the potential for EMI radiation.

Disadvantages: The primary disadvantage of differential circuitry is the increased number of traces. So, if none of the advantages are particularly significant in your application, differential signals and the associated routing considerations are not worth the cost in increased area. But if the advantages make a significant difference in the performance of your circuit, then increased routing area is the price we pay.

Impedance Issues: Differential traces couple into each other. This coupling affects the apparent impedance of the traces, and therefore the termination strategy employed (see Footnote 2 for a discussion on this issue and for suggestions on how to calculate differential impedance.) Calculating differential impedance is difficult. National Semiconductor has some references here, and Polar Instruments offers a standalone calculator (for a fee) that can calculate differential impedance for many different differential configurations[3]. High-end design packages also will calculate differential impedance.

But note that it is the coupling that *directly* affects the differential impedance calculation. The coupling between the differential traces must remain constant over the entire length of the trace(s) or there will be impedance continuities. This is the reason for the "constant spacing" design rule.

Footnotes:

1: See, for example, PCB Impedance Control", PC Design, March, 1998, and "What's All This Critical Length Stuff, Anyhow?" PC Design, October, 1999.

2: "Differential Impedance, What's the Difference," PC Design, August, 1998

3: See their web page at **http://www.polarinstruments.com/**

INSIDE DIFFERENTIAL SIGNALS

CADENCE COMMUNITY EDUCATIONAL SERIES – DECEMBER 2001

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WHY USE DIFFERENTIAL SIGNALS?

Differential signals can use lower voltage swings than are used with single-ended signals. This is possible because the differential threshold in a differential receiver is better controlled than the threshold of a single transistor. The lower swing leads to faster circuits and can reduce power consumption. Differential signaling also reduces EMI, since the opposite currents carried on the two traces leads to cancellation of the electric and magnetic fields at large distances. Similarly, differential signals are less sensitive to crosstalk. Some differential circuits use a complimentary single-ended signal, with the second half of the differential signal being taken from a voltage reference. This has the advantage of using a single trace for routing. The tradeoff is that this gives up some of the noise immunity available in a true differential signal.

WHAT IS A DIFFERENTIAL SIGNAL?

A differential signal is the difference between two signals. Wherever there is a differential signal, there will also be a common mode signal. LVDS signaling, for example, uses a 400 mV differential signal centered at 1.2V.

Figure 1 shows the simulation results for an LVDS interconnect. The top curves show the individual signals and the common mode signal; there is visible ringing on the common mode signal. The lower curve shows the differential signal, centered on 0 V.

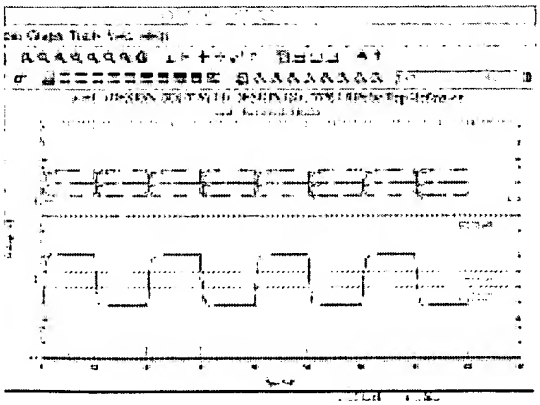

Figure 1: Individual signals and the differential signal for an LVDS interconnect.

The differential and common mode voltages can be expressed as:

Vdiff = (Vp – Vn)

Vcommon = (Vp + Vn)/2

A pair of transmission lines, each with impedance Z0, will have a different impedance for differential signals and for common mode signals. The differential impedance will depend on the spacing of the lines. If the lines are far apart (spacing >> width), then Zdiff = 2*Z0. As the lines are brought closer together, the coupling between the traces increases, and Zdiff decreases.

Both the differential signal and the common model signal will travel down the interconnects and suffer from reflections at impedance mismatches. The differential and common mode signals will behave differently, since they will see different effective impedances and different travel speeds down the transmission lines.

If the two traces carrying a differential signal are not routed side-by-side, there will be mixing of the common mode and differential mode parts of the signal. Near the driver, the common mode signal may be nearly zero. But near the receiver, if there is a significant delay difference, there may be a brief time when the differential signal is nearly zero. This is risky behavior, because the zero differential signal will be interpreted as a logical "0" or "1" by the receiver – and as long as the differential signal hovers near zero, the receiver can "oscillate", leading to multiple clock crossings or data oscillation. Both multiple clock crossings and data oscillation can be observed as system faults.

ASSIGNING DIFFERENTIAL DRIVER AND RECEIVERS

To keep a signal truly differential, the two driver pins should be as close as possible. They should use adjacent pins in the same IC to minimize any path differences. Package delays should also be matched; this requires having equal path lengths for traces within the package.

Drivers should be on the same power and ground rail sections within the IC; this makes power and ground bounce effects appear as common mode signals. At the other end of the signal path, the two receiver pins should also share a common power and ground rail pair, keeping the input logic thresholds the same for the two receivers and preserving the differential input threshold. If you are using single-ended differential input, the reference pin and input pins should have their own power and ground pins, separate from those used for the drivers, to minimize any bounce in the reference voltage.

Some differential drivers are nothing more than pairs of single-ended drivers on-chip, and are differential only in the sense that the logic value of the two is always opposite. Other differential drivers are coupled together on the chip, such that a change on one driver's current always causes a change in the other driver's current; an example of this is a differential-current mode driver.

The IBIS model can be used to associate a pair of pins. This allows you to explicitly define differential pin pairs for drivers and for receivers. Figure 2 shows an example of this assignment within an IBIS model. The IBIS model also allows definition of the differential threshold (equivalent to VMEAS or VTH for a single-ended signal), and the launch delay between the inverting and non-inverting signals for drivers.

[Diff Pin]		inv_pin	vdiff	tdelay_typ	tdelay_min	tdelay_max	
3	4	150mV	-1ns	0ns	-2ns		Input or I/O pair
7	8	0V	1ns	NA	NA		Output* pin pair
9	10	NA	NA	NA	NA		Output* pin pair
16	15	200mV	1ns				Input or I/O pin pair
20	19	0V	NA				Output* pin pair, tdelay = 0
22	21	NA	NA				Output*, tdelay = 0

Figure 2: IBIS differential pin section

ROUTING DIFFERENTIAL TRACE PAIRS

There are some routing rules that you can use to keep the differential signal differential. Violating these rules will cause part of the differential signal to become common mode, reducing the differential signal amplitude and increasing the common model signal amplitude.

Two of these rules have already been discussed: traces should be routed with equal delay, and crosstalk coupled nets should be routed to minimize differential crosstalk.

How does one route for equal delay? And how equal is equal, anyway? Depending on the edge rate of the differential signal, delays should be equalized to within 20% of the edge time or better to minimize the time the differential signal spends near the differential switching threshold. A good rule is to route the traces side-by-side, on the same layers. When changing layers, the two traces should change layers at the same location through the same number of vias, keeping the two signal paths as close together as possible.

To reduce crosstalk, differential pairs should never have any other traces routed between them. Simulation should be done to determine the minimum spacing to aggressor traces. This spacing will be different for a single-ended aggressor and for a differential aggressor pair.

Following a rule of thumb may allow you to get your design done, but it may also overconstrain your design. Simulation can be used to refine your rules of thumb, and to identify areas of the board where traces can be safely moved closer together. For example, crosstalk is an issue only when aggressor nets have fast edges; a slower edge signal may not present a crosstalk risk to your differential signal. Simulation and constraint checking can help you identify where routing rules can be relaxed.

TERMINATING DIFFERENTIAL TRACE PAIRS

It is difficult for high speed differential drivers to absorb reflections that are not differential, since the two halves of the differential signal have different turn-on times, edge rates, and driving impedances. They may also have different packaging parasitics. This means you cannot count on reflections to die out at the end of the first round trip.

The same rules apply to terminating differential pairs as you would use for other signal-carrying traces. If the trace length is longer than the critical length, then termination should be used. For a pure differential signal, a single terminating resistor between the two traces, of value 2*Z0, should work. In practice, it is usually necessary to also terminate the common mode signal. The common mode signal (or noise) is terminated by providing a terminator to ground (R or RC) from each line, or from the "center point" of a divided differential resistor.

SUMMARY

To make the most of differential signaling, remember to treat a differential signal as a single item. Any difference in the two halves of the signal converts part of the differential signal into undesirable common mode signal, leading to false clocks and data errors.

Drivers and receivers each need to be assigned to pins on the same IC. At high speeds, the package and pin assignment needs to match package delays. Driver assignment to power and ground rings on the chips must be checked to minimize the differential contribution of power and ground bounce. For single-ended differential signaling, receiver pins should not share a power or ground ring with any drivers.

The pair of traces needs to be routed together to maintain a matched delay. As edge rates drop below 1 nsec, this includes matching the number and location of vias, as well as matching layer assignments and lengths.

The best check on your differential design is simulation. Simulation and analysis in Cadence's SPECCTRAQuest can be used to check differential signals for signal integrity and timing issues. Performing both pre- and post-layout simulation ensures that your differential design intent can be captured in the form of design constraints and verified throughout the design process, from concept to product.

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